

PY32F032K2xT-START V2

User Guide



Puya Semiconductor (Shanghai) Co., Ltd

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1. Introduction

The PY32F032K2xT-START V2 development board integrates a PY-LINK emulator. For detailed usage instructions of PY-LINK, please refer to the document "PY-LINK OB_UserManual_EN.pdf". The START board uses the PY32F032K2xT as the main controller. This development board, equipped with a 32-bit ARM® Cortex®-M0+ CPU core from Puya, provides a simple hardware development environment. The board is powered via the USB interface of PY-LINK. It offers peripheral resources including extension pins, as well as SWD, Reset, User key, Reset key, LED, and more. This document provides detailed hardware schematics and related application examples.

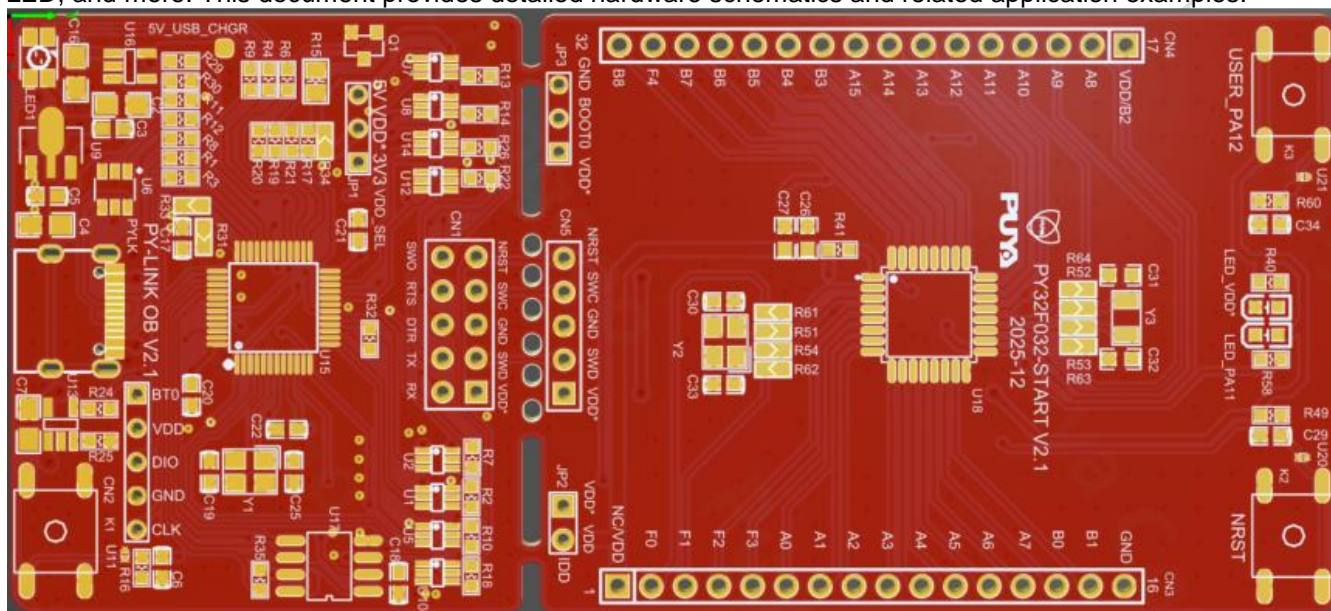


Figure 1-1 PCB 3D renderings

2. Functional pin assignment

Table 2-1 Pin Assignment

Function	Pin	Description	Note
LED	\	LED1	PY-LINK LED
	\	LED2	VDD*
	PA11	LED3	User LED
KEY	\	K1	PY-LINK Key
	PF2	K2	Reset Key
	PA12	K3	User Key
SPI	PA4	SPI_NSS	ExternalFLASH
	PB3	SPI_CLK	ExternalFLASH
	PB4	SPI_MISO	ExternalFLASH
	PB5	SPI_MOSI	ExternalFLASH

3. Overview of Hardware Design

The development board is powered via a Type-C USB connection. To download programs to the board, a Type-C USB cable is required. Select the correct boot mode, connect the USB cable, and if LED1 lights up, it indicates a proper power connection.

3.1 Power Supply

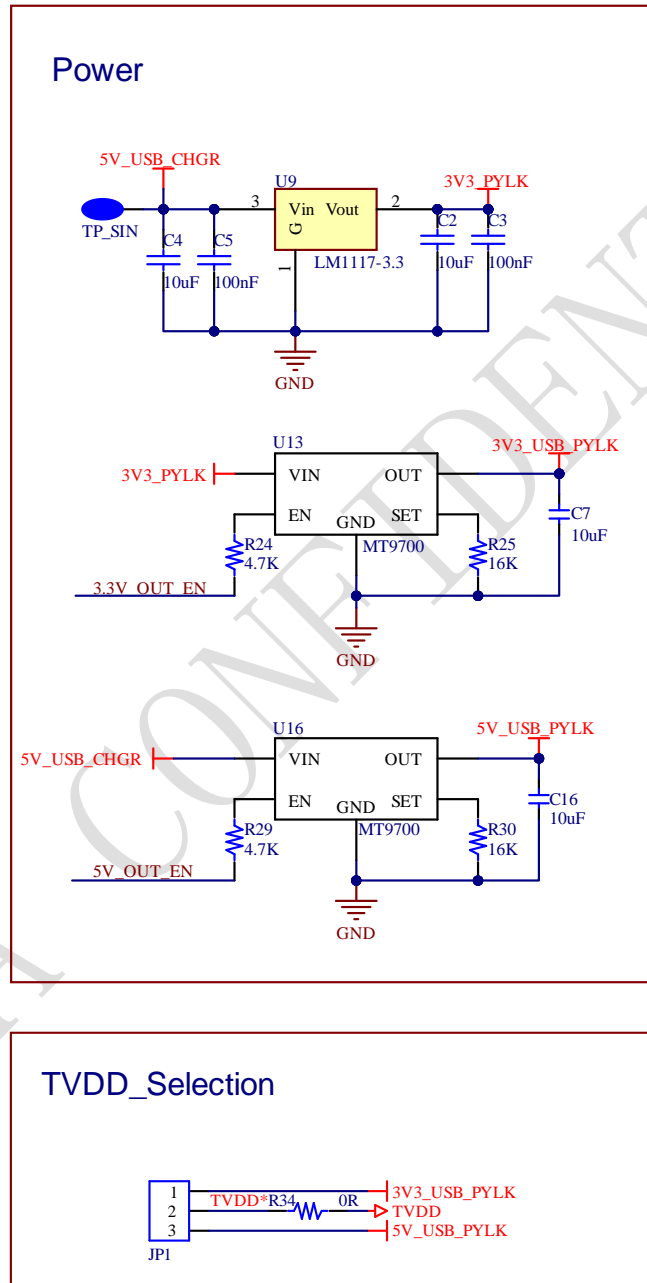


Figure 3-1 Power Supply Schematic

3.2 I_{DD} TEST

When JP2 OFF (symbol IDD) and R39 OFF, an ammeter can be connected to measure the power consumption of MCU.

JP2 OFF, R39 ON:MCU is powered. (Default setting and JP2 plug is not mounted before shipping)

JP2 ON, R39 OFF:MCU is powered.

JP2 OFF, R39 OFF:An ammeter must be connected. If there is no ammeter available, the MCU cannot be powered.

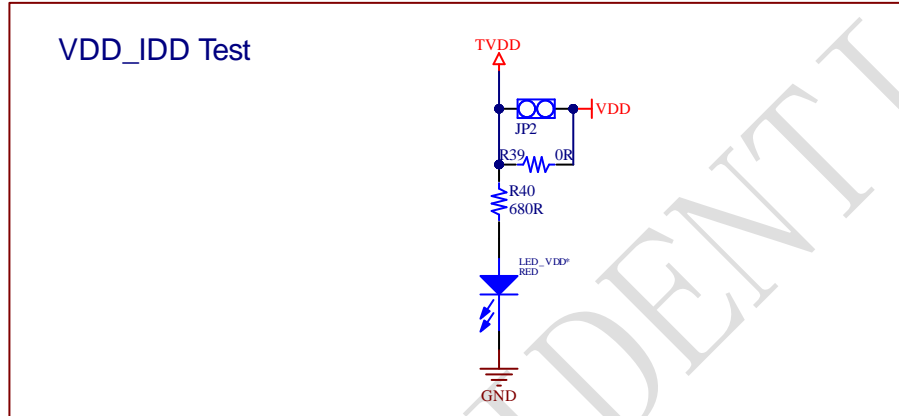


Figure 3-2 I_{DD} Schematic

3.3 LED Indicator Light

The red LED indicates that the board TVDD is powered as shown in the figure above; The green LED is the user LED connected to the PA11 pin of the MCU.

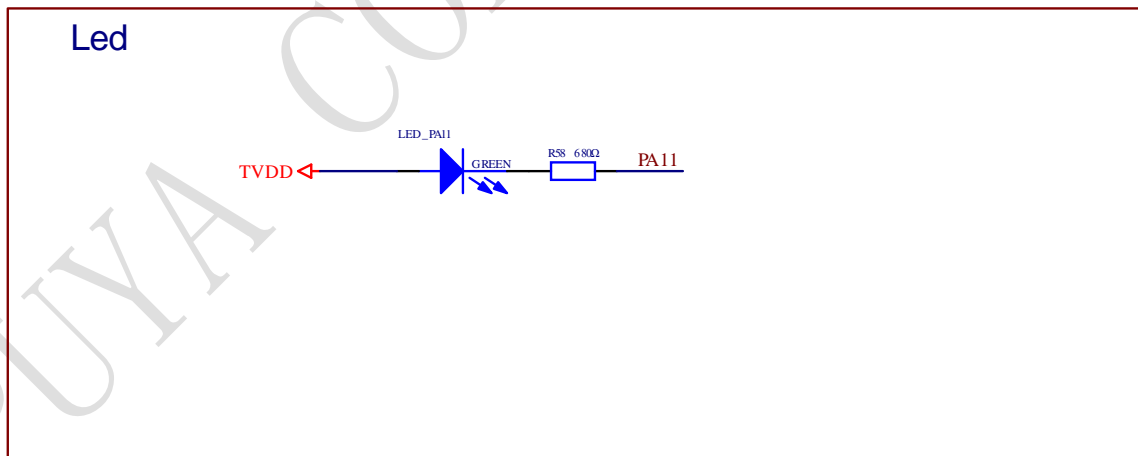


Figure 3-3 LED Schematic

3.4 Reset Key

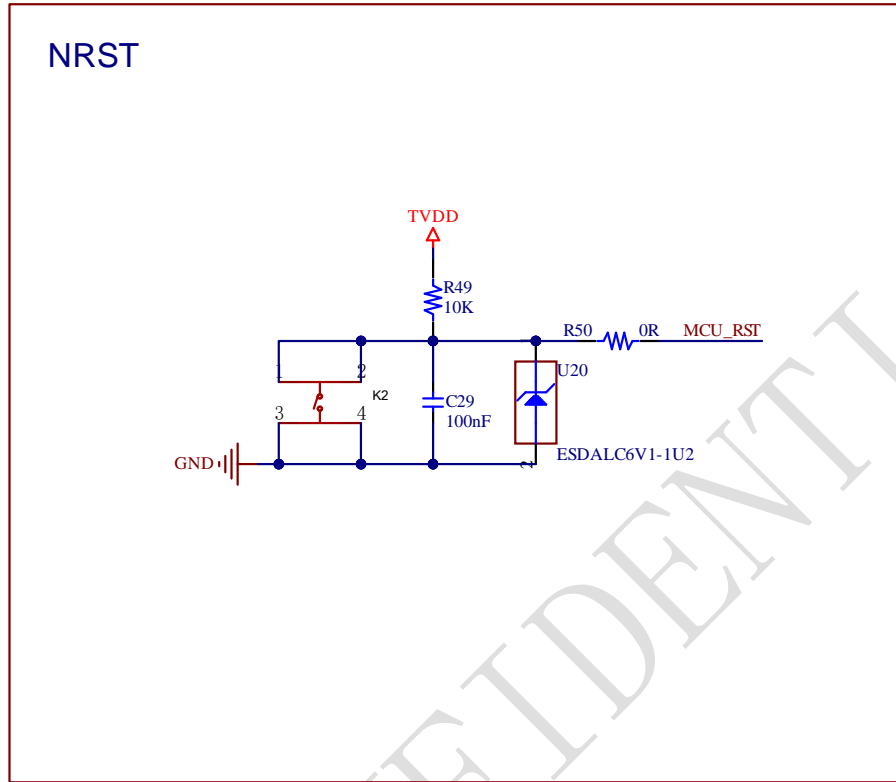


Figure 3-4 Reset Key Schematic

3.5 User Key

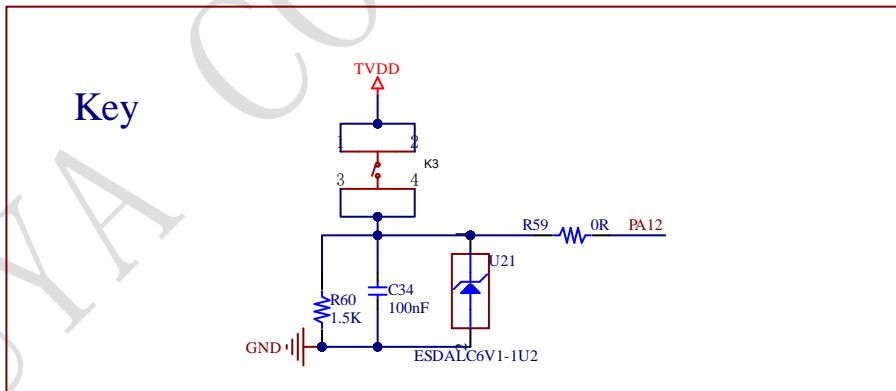


Figure 3-5 User Key Schematic

3.6 Boot Mode Selection

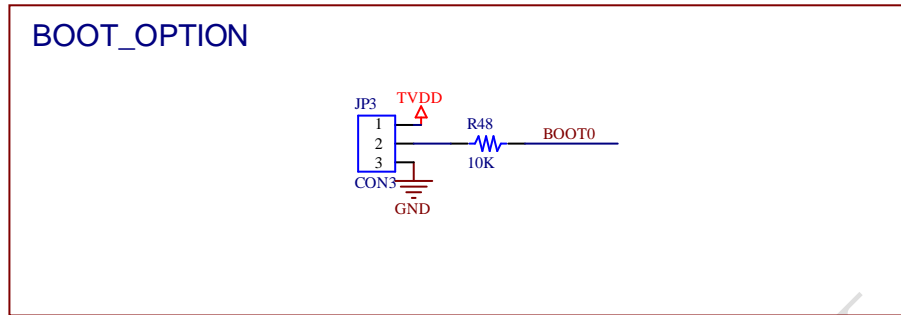


Figure 3-5 BOOT Mode Schematic

Three different boot mode can be selected through the nBOOT0/nBOOT1/BOOT_LOCK bits (stored in the Option bytes), as shown in the following table:

Table 3-6 Boot configuration

BOOT_LOCK	Boot mode configuration		Mode
	nBOOT1 bit	nBOOT0 bit	
1	X	X	Force boot from the Flash main store
0	X	0	Main Flash memory is selected as the boot area
0	1	1	System memory is selected as the boot area
0	0	1	Embedded SRAM is selected as the boot area

3.7 External Clock Source

HSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 24 MHz crystal is used as HSE clock source.

Oscillator from external PF0:

External oscillator is injected from the PF0 of CN3. The hardware must be configured: R51 OFF.

HSE unused

MCU PF0 and PF1 are used as GPIOs.

LSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 32.768 kHz crystal is used as HSE clock source.

Oscillator from external PA10:

External oscillator is injected from the PA10 of CN4. The hardware must be configured: R52 OFF.

LSE unused

MCU PA9 and PA10 are used as GPIOs.

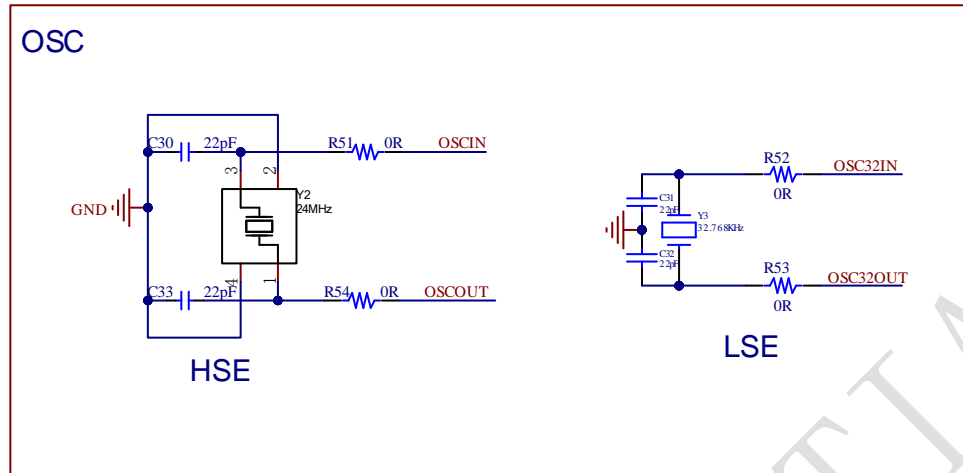


Figure 3-8 Clock source function schematic

3.8 Programming and debugging:

The evaluation board integrates PY-LINK for users to program/debug the PY32F032K2xT on the PY32F032K2xT-START V2 board. PY-LINK supports SWD interface mode, and supports a set of virtual serial ports (VCP) and PY32F032K2xT's USART1_TX/USART1_RX (PB6/PB7) to connect and communicate through Dupont wire, please refer <USART> to the official PY32xxxx_Firmware Example. For more information about PY-LINK operation, firmware upgrade, and precautions, please refer to the "PY-LINK OB_UserManual_EN.pdf" document. The PY-LINK on board can be disassembled or separated from the PY32F032K2xT-START V2. In this case, the PY32F032K2xT-START V2 can still be connected to the CN1 interface of PY-LINK through CN5 interface (not mounted before leaving factory), or to another PY-LINK, in order to continue to program and debug the PY32F032K2xT.

4. Guide to Using the Example

4.1 LED Example

Purpose of the Example

There is one LED on the development board, the LED is controlled by GPIO. This sample program will tell how to light up the LED.

Execution Results

Download the official PY32xxx_Firmware Example <GPIO_Toggle> to the board, reset and run, and the green LED flashes.

4.2 KEY Example

Purpose of the Example

There is 1 user button on the board. The user key is detected by the GPIO. This routine will show you how to detect a key with an external interrupt.

Execution Results

Download the official PY32xxx_Firmware Example <EXTI_IT> to the board, reset and run, press the button once, and the green LED will switch to the on-off state once.

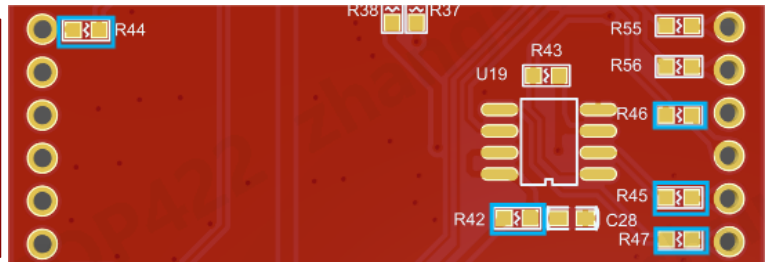
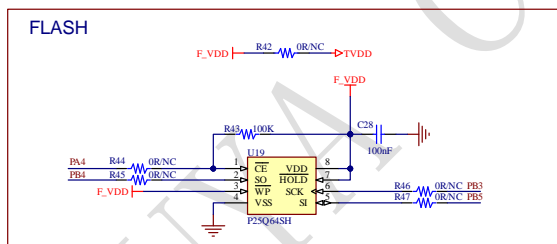
4.3 FLASH Example

Purpose of the Example

There is a flash on the development board, and the FLASH communication interface is connected to the SPI interface. This example will show you how to read and write FLASH via SPI.

Note:

1. To use this routine, the user needs to weld the 0R resistor at the position of R42, R44, R45, R46, and R47 by himself, and the specific position needs to be welded as shown in the figure below.
2. The maximum working voltage of FLASH is 3.6V. It is recommended that the supply voltage of TVDD should not exceed 3.3V.



Execution Results

Download the official PY32xxx_Firmware Example <SPI_FullDuplex_ExternalFLASH> to the board, reset and run. If the green LED is always on, the FLASH read and write is successful, otherwise the FLASH read and write fails.

5. Schematic

5.1 PY-LINK Schematic

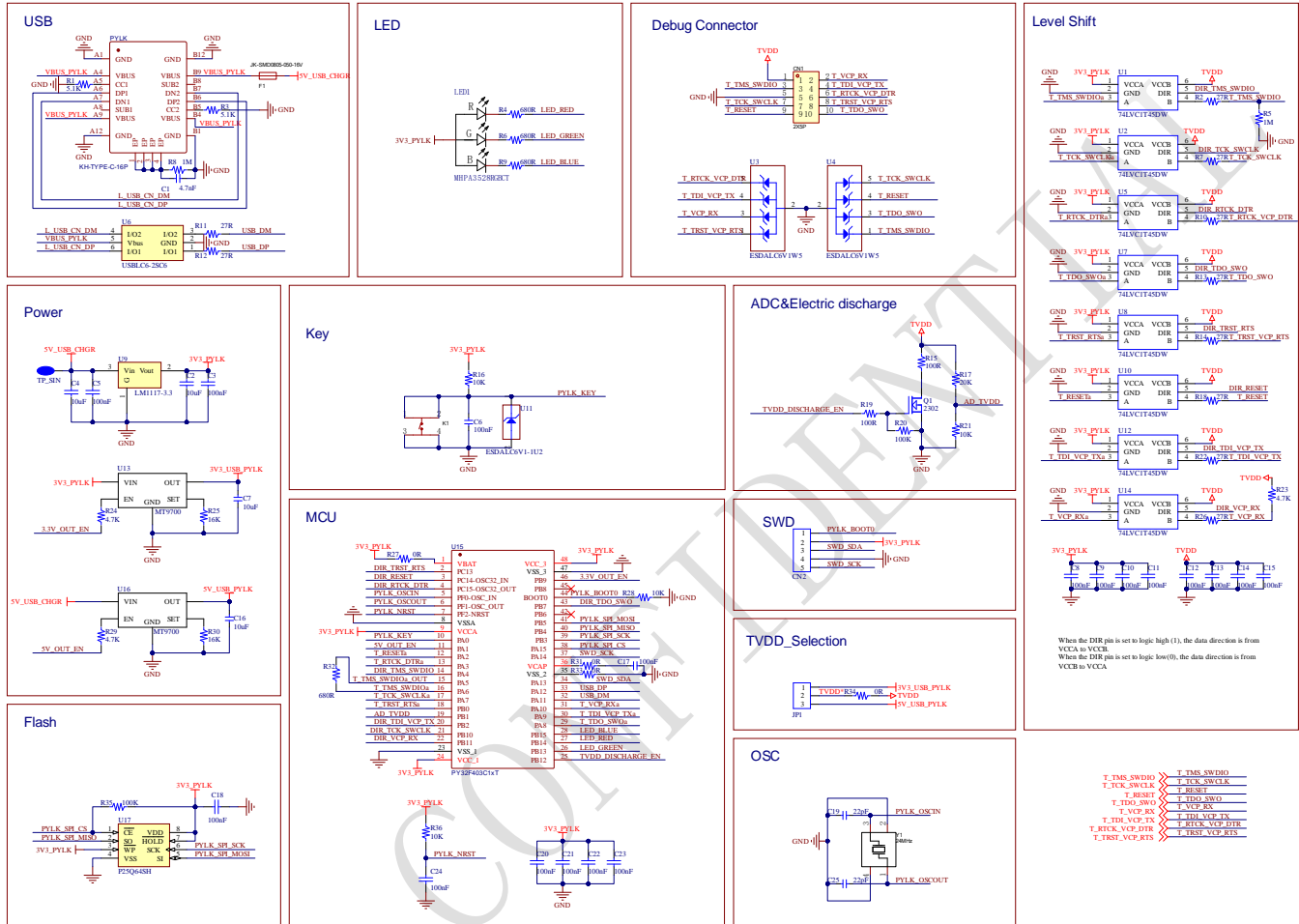
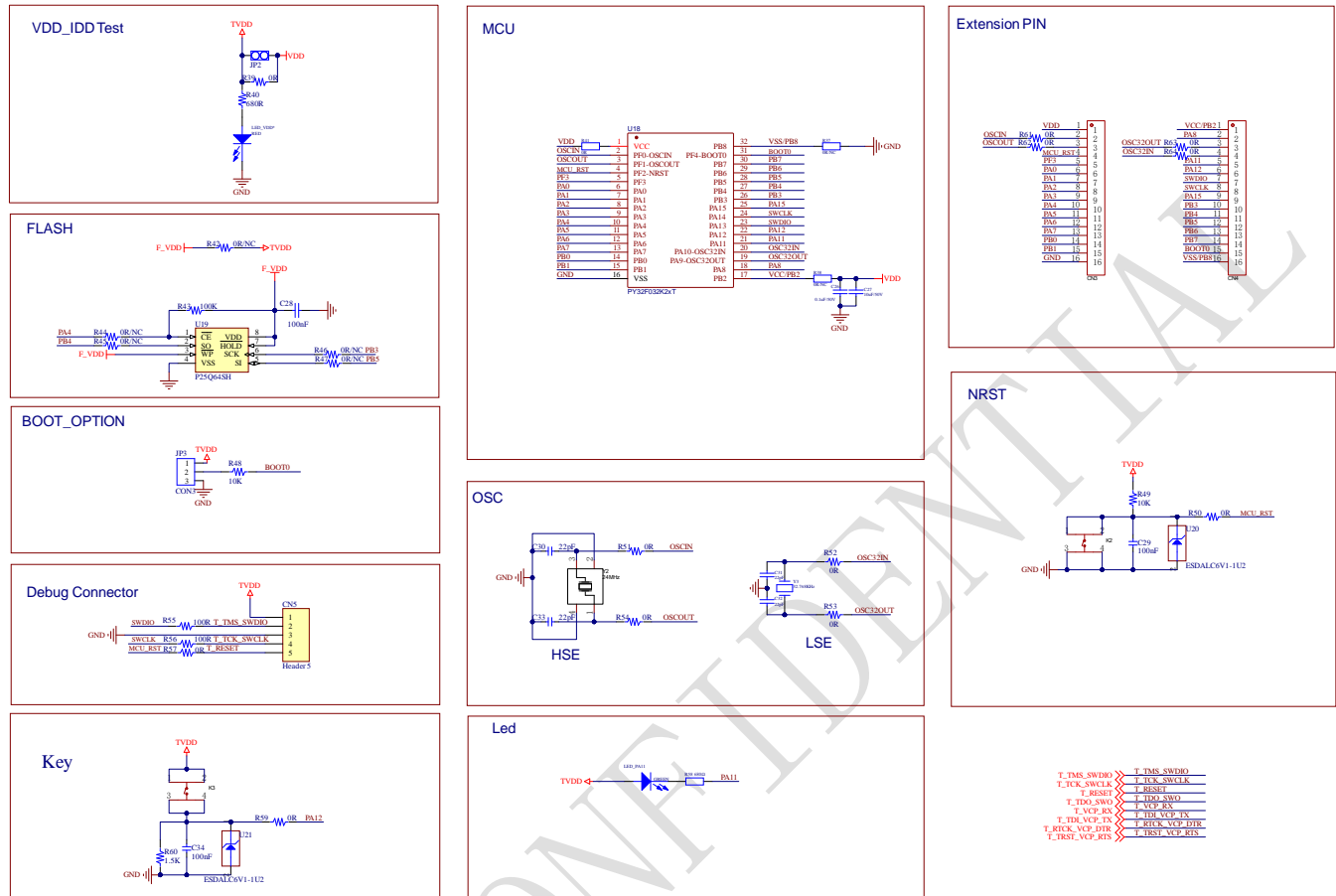


Figure 5-1 PY-LINK Schematic

5.2 MCU Schematic



6. Updated History

Version	Content	Date
V1.0	Initial version	2025/07/09
V1.1	Modified 3D renderings and MCU Schematic	2025/12/01



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